REMARKS

In the Office Action, claims 16-23 and 28-35 were rejected under 35 U.S.C. § 102(b) as being anticipated by USP 5,980,093 issued to Jones et al. (hereinafter "Jones"). Claims 24 and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Jones in view of USP 5,635,736 issued to Funaki et al. (hereinafter "Funaki"). Claims 25, 27, 37 and 39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Jones in view of USP 6,262,487 issued to Igarishi et al. (hereinafter "Igarishi"). Upon entry of this Amendment, no claims will be amended, cancelled or added. Claims 16-25, 27-37 and 39 will therefore be pending.

I. Rejection of Claims Under 35 U.S.C. § 102(b)

In the office action dated 05/21/2003, the Examiner rejected claims under 35 U.S.C. § 102(b). Specifically, the Examiner stated that the subject claims were anticipated by Jones et al. Applicants respectfully disagree with the Examiner's finding and accordingly traverse the rejection with arguments presented below.

A. Elements of Independent Claims 16 and 28

Independent claims 16 and 28 each contain a number of elements. Among those elements are "conductors deposed in a preferred Manhattan direction" in a first metal layer group and "a plurality of conductors deposed in a preferred diagonal direction" in a section adjacent to the first metal layer group. These elements are shown in the context of edited claims 16 and 28 presented below (emphasis added).

16. An integrated circuit comprising:

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a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising <u>conductors deposed in a preferred Manhattan direction</u>, ...

a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of the metal layer directly adjacent to said portion of said metal layer for said self contained layout section, ...

28. (Twice Amended) A method for deposing a plurality of metal layers comprising a plurality of conductors to interconnect components of an integrated circuit, said method comprising the steps of:

designating a first metal layer group comprising at least one metal layer, said metal layer in said first metal layer group comprising at least one self contained layout section comprising conductors deposed in a preferred Manhattan direction, ...

designating a second metal layer group comprising at least one metal layer, said metal layer in said second metal layer group comprising a plurality of conductors deposed in a preferred diagonal direction in a portion of the metal layer directly adjacent to said portion of said metal layer for said self contained layout, ...

Clearly, then, Jones must disclose the above-referenced elements in order to anticipate Applicants' invention.

B. The Examiner's Interpretation of Jones's Figure 7C

In rejecting claims in view of Jones, the Examiner pointed with particularity to Jones's Figure 7C. Element 106 of Figure 7C is characterized as a conductor deposed in a "preferred Manhattan direction." Furthermore, elements "B" and "C" of the figure are characterized as conductors deposed in a preferred diagonal direction in a portion of a metal layer directly adjacent to portion "A."

The Examiner's rejection is dependent upon the presence of the above-characterized elements in Figure 7C, as he did not point to other sections of Jones that provided the required elements of Applicants' claims 16 and 28.

C. The Examiner's Interpretation is Incorrect

Element 106 of Figure 7C is a pin, not a conductor (*i.e.*, wire). This is clearly described in Jones: "As shown therein, pins 102, 104, 106 and 108 are to be matched to pins 112, 114,

116, and 118 respectively." [Col. 9, lines 13-14] Applicants can only assume, therefore, that the conductor referred to by the Examiner is the line extending from 106 toward the left, bottom corner of the page. This line, according to the Examiner, is a conductor deposed in a Manhattan direction.

Applicants describe application of the terms "Manhattan" and "diagonal" to their invention on page 3 of the instant application. A "Manhattan direction" is one that runs horizontally or vertically in reference to the boundaries of a chip; a "diagonal direction" is one that does not run horizontally or vertically in reference to the boundaries of a chip. [Page 3, lines 4-8] In other words, a Manhattan direction cannot run parallel to a diagonal direction and *vice versa*.

Jones does not provide a relational reference (*e.g.*, relation to chip boundary) for his figures. It is accordingly difficult to understand the directionality of his depicted conductors. What is clear, however, is that the Examiner has characterized "conductor 106" as running in a Manhattan direction and "conductors B and C" as running in a diagonal direction. This is an incorrect characterization given that the line of 106 runs parallel to the lines of B and C. As pointed out in the preceding paragraph, a diagonal line CANNOT run parallel to a Manhattan one.

Applicants further respectfully note that the Examiner has misinterpreted his elements "B" and "C" of Figure 7C. The Examiner has characterized these elements as conductors (*i.e.*, wires), which is not correct. According to Jones, lines B and C are potential grids used for routing, not conductors:

> Initially, the first thread plans the connection for the first pin pair 102-112, the second pin plans the connection for the second pin pair 104-114, and the third thread plans the connection between the third pin pair 106-116. The three threads are not shown. In actual operation, a thread handles more than a single pin pair and pins may be associated in groups larger than two, but for purposes of

> illustration it is assumed that each thread handles a single pin pair at a time. A partial routing, after stepping through wiring for potential planned paths, is shown in FIG. 7B. Potential grids as planned by the second thread are illustrated as reserved grids 120, and other grids cannot plan into reserved grids 120. Pin pair 108-118 have neither been planned nor routed. FIG. 7C illustrates completion of first pin pair 102-112 by the first thread, at which point the first thread begins to plan and route fourth pin pair 108-118. [Col. 9, lines 19-34, emphasis added]

Therefore, Figure C does not disclose conductors (*i.e.*, "B" and "C") deposed in a preferred diagonal direction in a portion of a metal layer directly adjacent to portion "A," as thought be the Examiner.

D. The Rejection Under 35 U.S.C. § 102(b) Should Be Withdrawn

Since Jones does not disclose all the elements of Applicants' invention (arguments presented above), Jones cannot be used to support a rejection of claims 16-23 and 28-35 under 35 U.S.C. § 102(b). Respectfully, therefore, the rejection should be withdrawn.

II. Rejection of Claims Under 35 U.S.C. § 103(a)

In the office action dated 05/21/2003, the Examiner rejected claims 24, 25, 27, 36, 37 and 39 under 35 U.S.C. § 103(a). Specifically, the Examiner rejected claims 24 and 36 as being unpatentable over Jones in view of Funaki; claims 25, 27, 37 and 39 were rejected over Jones in view of Igarishi. Applicants respectfully contend that a *prima facie* case of obviousness has not been made for the referenced claims. At the very least, since Jones does not teach or suggest all the elements of independent claims 16 and 28 (see arguments presented above), and since neither Funaki nor Igarishi make up for this deficiency, then the following standard has not been met:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. [MPEP 2143, emphasis added]

CONCLUSION

In view of the foregoing, it is submitted that the claims are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

STATTLER, JOHANSEN & ADELI LLP

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Jeffrey A. McKinney

Reg. No. 43,795

Stattler Johansen & Adeli LLP
PO Box 51860
Palo Alto, CA 94303-0728
Phone: (650) 752-0990 ext.103
Fax: (650) 752-0995